

MULTILAYER CERAMIC CHIP CAPACITORS

Ordering Code

CC 0805 Y 104 Z 160
 (1) (2) (3) (4) (5) (6)

(1)

Style
CC : MLCC

(3)

Dielectric Material
N : NP0
X : X7R
Y : Y5V
Z : Z5U
U : Y5U
B : X5R
S : X6S

(2)

Chip Size: L×W
0201=0.02×0.01"
0402=0.04×0.02"
0603=0.06×0.03"
0805=0.08×0.05"
1206=0.12×0.06"
1210=0.12×0.10"
1808=0.18×0.08"
1812=0.18×0.12"

(4)

Capacitance
in pF, the first two digits are significant digits and the last digits gives the no. of zeros.
Example :
0=x1 270=27pF
1=x10 271=270pF
2=x100 272=2.7nF
3=x1000 273=27nF
4=x10000 274=270nF
5=x100000 275=2.7 μF
6=x1000000 276=27 μF

(5)

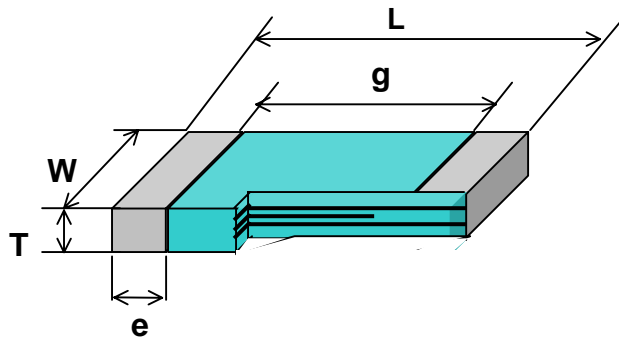
Tolerance
A: ±0.05pf H: ±3%
B: ±0.10pf J: ±5%
C: ±0.25pf K: ±10%
D: ±0.50pf M: ±20%
F: ±1% Z: +80/-20%
G: ±2% E: ±1pf
Note: A,B,C,D: for <10pF
NPO: ALL
Tolerance
X7R/X5R: J,K,M
Z5U/Y5V/Y5U : M,Z

(6)

Rated Voltage
16V=160
25V=250
50V=500
100V=101
200V=201
500V=501
1KV=102
3KV=302
10V=100
250V=251
2KV=202
63V=630
630V=631

MULTILAYER CERAMIC CHIP CAPACITORS

Chip Capacitor Structure & dimension



Size	L Length inch (mm)	W Width inch (mm)	e Termination inch (mm)	g(min) Insulation inch (mm)
0402	0.04±0.002 (1.0±0.05)	0.02±0.002 (0.5±0.05)	0.0059~0.0118 (0.15~0.3)	0.0157 (0.4)
0603	0.063±0.004 (1.6±0.1)	0.032±0.003 (0.8±0.1)	0.0079~0.0196 (0.2~0.5)	0.0196 (0.6)
0805	0.079±0.006 (2.0±0.15)	0.049±0.006 (1.25±0.15)	0.0098~0.0276 (0.25~0.65)	0.0591 (0.7)
1206 (C<10uF)	0.126±0.006 (3.2±0.15)	0.063±0.006 (1.6±0.15)	0.0098~0.0295 (0.25~0.75)	0.0787 (1.7)
1206 (C 10uF)	0.126±0.008 (3.2±0.2)	0.063±0.008 (1.6±0.2)	0.0098~0.0295 (0.25~0.75)	0.0787 (1.7)
1210	0.126±0.012 (3.2±0.3)	0.098±0.008 (2.5±0.2)	0.0118~0.0295 (0.3~0.75)	0.0787 (1.7)
1808	0.177±0.012 (4.5±0.3)	0.079±0.008 (2.0±0.2)	0.0098~0.0381 (0.25~0.97)	0.1176 (2.5)
1812	0.177±0.012 (4.5±0.3)	0.126±0.008 (3.2±0.2)	0.0098~0.0381 (0.25~0.97)	0.1176 (2.5)

	Code	Thickness
0402	S	0.50mm±0.05mm
0603	S	0.80mm±0.10mm
0805/1206	A	0.6 mm±0.1mm
0805/1206	B	0.8 mm±0.1mm
0805/1206/1210	C	1.0 mm±0.1mm
0805/1206/1210/1812	D	1.15 mm±0.1mm
0805/1206/1210/1812	E	1.25 mm±0.1mm
1206 ^{Note1} /1210/1808/1812	F	1.60 mm±0.15mm
1210/1812	G	1.90 mm±0.15mm
1210/1812	H	2.10 mm±0.15mm
1210	T	> 2.25mm (Max2.8mm)
1812	T	> 2.25mm (Max3.2mm)
0805/1206	K	< 0.6mm

*Note1: For 1206 size, If C 10uF, the thickness is 1.70 mm±0.2mm

MULTILAYER CERAMIC CHIP CAPACITORS

Product Range

(Product size above 0603 may have several thickness range, the max thickness was shown on the following table for reference)

CLASS	Class II													
T.C.	X7R													
TYPE														
SIZE	0402				0603					0805				
RV	10V	16V	25V	50V	6.3V	10V	16V	25V	50V	6.3V	10V	16V	25V	50V
22P	S	S	S	S	S	S	S	S	S					
27P	S	S	S	S	S	S	S	S	S					
47P	S	S	S	S	S	S	S	S	S					
100P	S	S	S	S	S	S	S	S	S		B	B	B	B
120P	S	S	S	S	S	S	S	S	S		B	B	B	B
150P	S	S	S	S	S	S	S	S	S		B	B	B	B
180P	S	S	S	S	S	S	S	S	S		B	B	B	B
200P	S	S	S	S	S	S	S	S	S		B	B	B	B
220P	S	S	S	S	S	S	S	S	S		B	B	B	B
270P	S	S	S	S	S	S	S	S	S		B	B	B	B
330P	S	S	S	S	S	S	S	S	S		B	B	B	B
390P	S	S	S	S	S	S	S	S	S		B	B	B	B
470P	S	S	S	S	S	S	S	S	S		B	B	B	B
560P	S	S	S	S	S	S	S	S	S		B	B	B	B
680P	S	S	S	S	S	S	S	S	S		B	B	B	B
820P	S	S	S	S	S	S	S	S	S		B	B	B	B
1.0n	S	S	S	S	S	S	S	S	S		B	B	B	B
1.2n	S	S	S	S	S	S	S	S	S		B	B	B	B
1.5n	S	S	S	S	S	S	S	S	S		B	B	B	B
1.7n	S	S	S	S	S	S	S	S	S		B	B	B	B
1.8n	S	S	S	S	S	S	S	S	S		B	B	B	B
1.8n	S	S	S	S	S	S	S	S	S		B	B	B	B
2.2n	S	S	S	S	S	S	S	S	S		B	B	B	B
2.7n	S	S	S	S	S	S	S	S	S		B	B	B	B
3.3n	S	S	S	S	S	S	S	S	S		B	B	B	B
3.9n	S	S	S	S	S	S	S	S	S		B	B	B	B
4.7n	S	S	S	S	S	S	S	S	S		B	B	B	B
5.6n	S	S	S	S	S	S	S	S	S		B	B	B	B
6.8n	S	S	S	S	S	S	S	S	S		B	B	B	B
8.2n	S	S	S	S	S	S	S	S	S		B	B	B	B
10n	S	S	S	S	S	S	S	S	S		B	B	B	B
12n	S	S	S	S	S	S	S	S	S		B	B	B	B
15n	S	S	S	S	S	S	S	S	S		B	B	B	B
18n	S	S	S	S	S	S	S	S	S		B	B	B	B
22n	S	S	S	S	S	S	S	S	S		B	B	B	B
27n	S	S	S	S	S	S	S	S	S		B	B	B	B
33n	S	S	S	S	S	S	S	S	S		B	B	B	B
39n	S	S	S	S	S	S	S	S	S		B	B	B	B
47n	S	S	S	S	S	S	S	S	S		B	B	B	B
56n	S	S	S	S	S	S	S	S	S		B	B	B	B
68n	S	S	S	S	S	S	S	S	S		B	B	B	E
82n	S	S	S	S	S	S	S	S	S		B	B	B	B
100n	S	S	S	S	S	S	S	S	S		B	B	E	B
120n	S	S	S	S	S	S	S	S	S		B	B	E	B
150n	S	S	S	S	S	S	S	S	S		B	B	E	B
180n	S	S	S	S	S	S	S	S	S		D	B	E	B
220n	S	S	S	S	S	S	S	S	S		D	E	E	E
270n	S	S	S	S	S	S	S	S	S		B	B	E	B
330n	S	S	S	S	S	S	S	S	S		E	E	E	E
390n	S	S	S	S	S	S	S	S	S		E	E	E	E
470n	S	S	S	S	S	S	S	S	S		E	E	E	E
560n	S	S	S	S	S	S	S	S	S		E	E	E	E
680n	S	S	S	S	S	S	S	S	S		D	E	E	E
820n	S	S	S	S	S	S	S	S	S		E	E	E	E
1.0u	S	S	S	S	S	S	S	S	S	E	E	E	E	E
1.2u	S	S	S	S	S	S	S	S	S		E	E	E	E
1.5u	S	S	S	S	S	S	S	S	S		E	E	E	E
1.8u	S	S	S	S	S	S	S	S	S		E	E	E	E
2.2u	S	S	S	S	S	S	S	S	S		E	E	E	E
4.7u	S	S	S	S	S	S	S	S	S		E	E	E	E
10u	S	S	S	S	S	S	S	S	S		E	E	E	E

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Product Range

(Product size above 0603 may have several thickness range, the max thickness was shown on the following table for reference)

CLASS	Class II																							
T.C.	X5R																							
TYPE																								
SIZE	0402			0603				0805				1206				1210				1812				
RV	6.3V	10V	16V	6.3V	10V	16V	25V	6.3V	10V	16V	25V	6.3V	10V	16V	25V	6.3V	10V	16V	25V	6.3V	10V	16V	25V	
100P																								
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27n		S	S																					
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47n		S	S																					
56n		S					S																	
68n		S					S																	
82n		S					S																	
100n	S	S					S																	
120n	S					S	S																	
150n	S					S	S																	
180n	S					S	S																	
220n	S			S	S	S																		
270n				S	S	S																		
330n				S	S	S																		
390n																								
470n	S			S	S	S																		
560n				S	S															E				
680n				S	S					E										E				
820n				S	S															E				
1.0u	S			S	S	S		E	E	E														
1.2u				S																				
1.5u				S																				
1.8u				S																				
2.2u				S				D	E										D					
3.3u									E										F					
4.7u				S				E	E									F	F	F				T
10u								E				G	F	G	F			G	H	T				F
22u								E				G						T		T				

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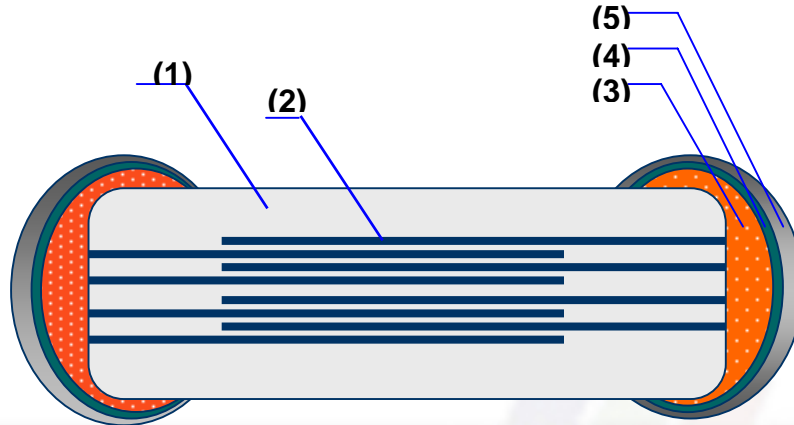
Product Range

(Product size above 0603 may have several thickness range, the max thickness was shown on the following table for reference)

CLASS	Class II											
T.C.	Y5V											
TYPE												
SIZE	1206						1210					1812
RV	6.3V	10V	16V	25V	35V	50V	10V	16V	25V	35V	50V	
10n		B	B	B	B	B						
12n		B	B	B	B	B						
15n		B	B	B	B	B						
18n		B	B	B	B	B						
22n		B	B	B	B	B						
27n		B	B	B	B	B						
33n		B	B	B	B	B						
39n		B	B	B	B	B						
47n		B	B	B	B	B						
56n		B	B	B	B	B						
68n		B	B	B	B	B						
82n		B	B	B	B	B						
100n		B	B	B	B	B	D	D	D	D	D	
120n		B	B	B	B	B	D	D	D	D	D	
150n		B	B	B	B	B	D	D	D	D	D	
180n		B	B	B	B	B	D	D	D	D	D	
220n		B	B	B	B	B	D	D	D	D	D	
270n		B	B	B	B	B	D	D	D	D	D	
330n		B	B	B	B	B	D	D	D	D	D	
470n		B	B	B	B	B	D	D	D	D	D	
680n		C	C	C	D	D	D	D	D	D	D	
1.0u		C	D	D	D	D	D	D	D	D	D	
1.2u		D	D	D			D	D	D	D	D	
1.5u		D	D	D			D	D	D	D	D	
1.8u		D	D	D			D	D	D	D	D	
2.2u		D	D	D	E	E	D	D	D	D	D	
2.7u		D	D				D	D	D			
3.3u		D	D	E			D	D	D			
3.9u		D	D				D	D	D			
4.7u		F	F	F	F		D	D	F			
5.6u		F					D	D				
6.8u		F					D	D				
8.2u		F					D	D				
10u		F	F				D	H	F	F		
12u							G					
15u							G					
18u							G					
22u		F	F				G	G				
47u	F						G					

MULTILAYER CERAMIC CHIP CAPACITORS

Inside structure and material



No.	Name	Material	
		Class 1	Class 2
(1)	Dielectric	TiO ₂	BaTiO ₃
(2)	Electrode	Ag/Pd or Ni	
(3)	Termination	Ag or Ag/Pd or Cu	
(4)		Ni	
(5)		Sn	

MULTILAYER CERAMIC CHIP CAPACITORS

Dielectric Material

Material	Tolerance	Characteristics	Application
NPO (COG)	1) A,B,C,D,E,F,G 2) J,K preferred	Class I Low K dielectric : extremely stable in capacitance regardless of time and temperature change, With low dielectric loss and small tolerance on nominal capacitance.	Precision timing circuits, high frequency noise filtering impedance matching, ESD Limiting.
X7R X5R	1) J 2) K,M preferred	Class II middle K dielectric: allowing higher capacitance than Class I dielectric in less stable frequency, voltage, and temperature condition.	Noise filtering, frequency discrimination, by-pass and decoupling in radio receivers, audio tone, and computer serve system.
Z5U Y5V Y5U	1) M,Z preferred	Class II High K dielectric: allowing high capacitance density as a replacement of tantalum, aluminum electrolytic capacitor.	Low frequency noise by-pass and high speed power decoupling application.

Capacitor Classification

Classification of ceramic based capacitor

By refer to EIA standard, ceramic capacitors are break down into three categories:

CLASS I: COG(NPO), also called “temperature compensation” type, It is temperature stable or compensating device, it shows very little or no changes in capacitance as temperature change, suitable for timing, impedance matching, ESD/EMI limiting.

CLASS II: X7R,X5R,Z5U,Y5V, also called “high K” type, those material present greater capacitance change than class I type, a variety of dielectric materials are available thus the amount of capacitance change is to be defined from vendor to vendor.

CLASS III: is semiconductor type which exhibit capacitance change similar to class II, however, this type is very rare in consumer application.

MULTILAYER CERAMIC CHIP CAPACITORS

Aging Phenomenon

What is aging of class II ceramic (change of capacitance over time)

Aging is the Shelf-Loss in capacitance that occurs over time and is a normal process of class II ceramic capacitors, because of the re-ordering of crystalline structure

When a class II ceramic body is cool from its Curie Point @150 and without voltage applied, then the aging starts under a given ratio designated by vendor.

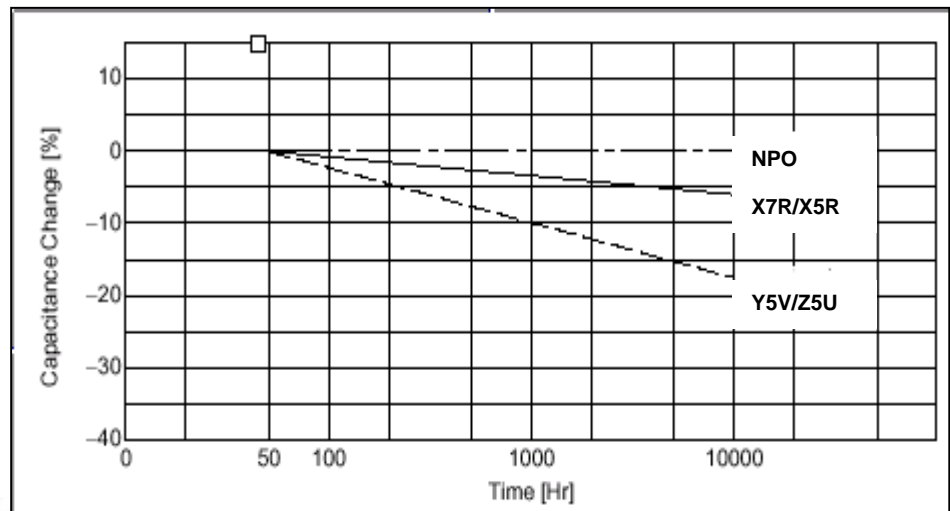
The average aging ratio (per 10^x time decade)

NPO 0

X7R/X5R 2.5%

Z5U 5%

Y5V/Y5U 7%



Recovery of aging

- 1) heat up to device at 150 or above, the higher temperature the less time required.
- 2) Voltage slows very much the aging behaviors of class II ceramic capacitor.

Handle guidelines of aging part

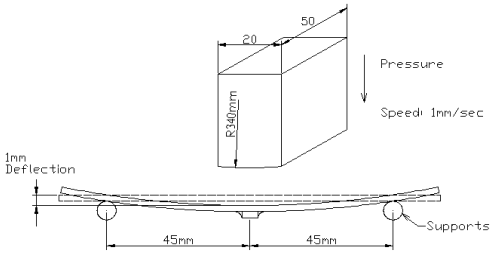
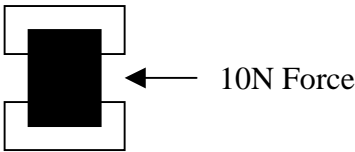
- 1) The aging parts will not lead to any reliability issue, but capacitance out from its lower limit which might be observed prior to production.
- 2) After de-aging process, the parts would back to its initial designated level of capacitance characteristic and another aging cycle begins when parts putting back to the storage shelf.
- 3) Typically, a process of IR-reflow or wave soldering can easily re-cure the aging part since it all working at much higher temperature than 150, even few seconds dwelling time is far enough for staying at such 210 ~260 range.
- 4) Re-measurement of de-aging parts, must to wait at least 24 hours at room temperature. While the part has cool down, then the capacitance is stable and shall be well within its normal limit.

MULTILAYER CERAMIC CHIP CAPACITORS

TESTS AND REQUIREMENTS

Item	Condition of test	Performance of requirement																					
Operating Temperature		NPO:-55 ~125 X7R:-55 ~125 X5R:-55 ~85 Z5U:+10 ~85 Y5V/Y5U:-30 ~85																					
Capacitance	NPO: 1000pF,F=1MHz,V=1.0±0.2Vrms > 1000pF,F=1KHz,V=1.0±0.2Vrms X7R/X5R/Y5V/Y5U/Z5U F=1KHz,V=1.0V±0.2Vrms	Within specified tolerance																					
Dissipation Factor	Same condition as capacitance.	NPO: Cap 30pF, Q 1000 Cap < 30pF, Q 400 + 20C																					
		X7R/ X5R: Rate Voltage 50V: 2.5% Rate Voltage 25V: 3.0% (C<1uF) Rate Voltage 16V: 3.5% (C<1uF) ^{<Note>} <Note>: For 0402 size, C=0.1uF, D.F 5% Rate Voltage 25V,16V: 5% (C 1uF) Rate Voltage 10V: 5% Rate Voltage 6.3V: 7%																					
		Z5U: All 3.5%																					
		Y5V/ Y5U: Rate Voltage 50V: 5% Rate Voltage 25V: 7% Rate Voltage 16V: 9% Rate Voltage 10V: 12.5%																					
Withstanding Voltage	DC voltage 250% of the rated voltage is applied between the terminations for 1 to 5 seconds, the charge and discharge current is less than 50mA.	No mechanical breakdown																					
Insulation resistance	Applying the rated voltage for 1 minute.	100G or 500 F MIN., whichever is smaller.																					
Temperature coefficient	With no electrical load, using the capacitance measured in step 3 as a reference. Then cycling the temperature sequentially from step 1 to 5.	<table border="1"> <thead> <tr> <th>Char.</th> <th>Temp. range.</th> <th>Cap. Change</th> </tr> </thead> <tbody> <tr> <td>NPO</td> <td>-55~+125</td> <td>±30PPM/</td> </tr> <tr> <td>X7R</td> <td>-55~+125</td> <td>±15%</td> </tr> <tr> <td>X5R</td> <td>-55~85</td> <td>±15%</td> </tr> <tr> <td>Z5U</td> <td>+10~+85</td> <td>+22%~-56%</td> </tr> <tr> <td>Y5V</td> <td>-30~+85</td> <td>+22%~-82%</td> </tr> <tr> <td>Y5U</td> <td>-30~+85</td> <td>+22%~-56%</td> </tr> </tbody> </table>	Char.	Temp. range.	Cap. Change	NPO	-55~+125	±30PPM/	X7R	-55~+125	±15%	X5R	-55~85	±15%	Z5U	+10~+85	+22%~-56%	Y5V	-30~+85	+22%~-82%	Y5U	-30~+85	+22%~-56%
		Char.	Temp. range.	Cap. Change																			
NPO	-55~+125	±30PPM/																					
X7R	-55~+125	±15%																					
X5R	-55~85	±15%																					
Z5U	+10~+85	+22%~-56%																					
Y5V	-30~+85	+22%~-82%																					
Y5U	-30~+85	+22%~-56%																					
<table border="1"> <thead> <tr> <th>Step</th> <th>Temperature</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>25±2</td> </tr> <tr> <td>2</td> <td>Min. operating temp.±3</td> </tr> <tr> <td>3</td> <td>25±2</td> </tr> <tr> <td>4</td> <td>Max. operating temp.±3</td> </tr> <tr> <td>5</td> <td>25±2</td> </tr> </tbody> </table>	Step	Temperature	1	25±2	2	Min. operating temp.±3	3	25±2	4	Max. operating temp.±3	5	25±2											
Step	Temperature																						
1	25±2																						
2	Min. operating temp.±3																						
3	25±2																						
4	Max. operating temp.±3																						
5	25±2																						

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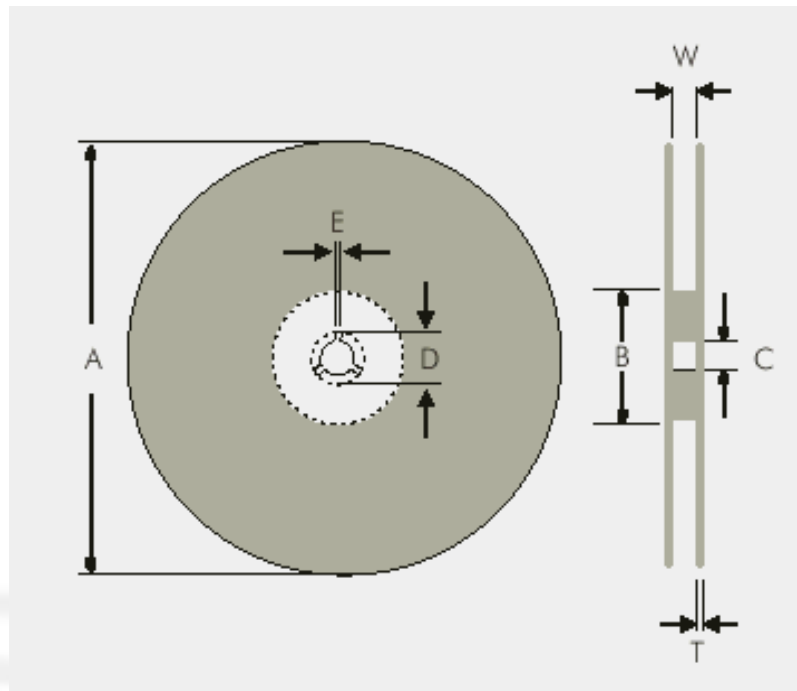
Item	Condition of test	Performance of requirement															
Solderability	Soldering temperature :235±5 Immersion time: 2±1 sec	At least 95% of the terminal surface must be covered by new solder.															
Resistance to soldering heat	Preheat the capacitor at 120~150 for 1 minute. Immerse the capacitor in a eutectic solder solution at 260±5 for 10±0.5 seconds. Measurement to be made after keeping at room temperature for 24±2 hrs of class 1part;for 48±4 hrs of class 2 part.	C/C: NPO: ±2.5% or 0.25pF max. Whichever is larger. X7R/X5R: ±7.5% max. Y5V/Y5U/Z5U: ±20% max. DF, I.R, Withstanding Voltage : To meet initial requirement. No remarkable damage															
Temperature cycle	Perform the five cycles according to the four heat treatments listed in the following table. <table border="1" data-bbox="322 792 940 1041"> <thead> <tr> <th>Step</th> <th>Temperature</th> <th>Time</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>Min. operating temp.±3</td> <td>30±3 min.</td> </tr> <tr> <td>2</td> <td>25±2</td> <td>2~3 min.</td> </tr> <tr> <td>3</td> <td>Max. operating temp.±3</td> <td>30±3 min.</td> </tr> <tr> <td>4</td> <td>25±2</td> <td>2~3 min.</td> </tr> </tbody> </table> Measurement to be made after keeping at room temperature for 24±2 hrs of class 1part;for 48±4 hrs of class 2 part.	Step	Temperature	Time	1	Min. operating temp.±3	30±3 min.	2	25±2	2~3 min.	3	Max. operating temp.±3	30±3 min.	4	25±2	2~3 min.	C/C: NPO: ±2.5% or 0.25pF max. Whichever is larger. X7R/X5R: ±7.5% max. Y5V/Y5U/Z5U: ±20% max. DF, I.R, Withstanding Voltage : To meet initial requirement. No remarkable damage
Step	Temperature	Time															
1	Min. operating temp.±3	30±3 min.															
2	25±2	2~3 min.															
3	Max. operating temp.±3	30±3 min.															
4	25±2	2~3 min.															
Deflection	Bending 1mm at a rate of 1mm/s, radius jig340mm.Capacitance be measured at deflection 1mm condition and then the pressure shall be maintained for 5±1 sec. 	C/C: NPO: ±5% or ±0.5pF Max., Whichever is larger. X7R/X5R: ±10% Y5V/Y5U/Z5U: ±20% No remarkable damage															
Adhesion	Solder the capacitor to circuit board. Then apply a 1kg(10N) force for 10±1 sec., refer to below figure.  Note: For 0402 type, apply 0.5kg(5N) Force.	No removal of the terminations or other defects shall occur.															

MULTILAYER CERAMIC CHIP CAPACITORS

Item	Condition of test	Performance of requirement
<p>Damp heat</p>	<p>Apply the rated voltage for 1000+24/-0 hours at 40±2 and 90 to 95% RH.</p> <p>Measurement to be made after keeping at room temperature for 24±2 hrs of class 1 part; for 48±4 hrs of class 2 part.</p>	<p>C/C: NPO: ±7.5% or ±0.75pF max. Whichever is larger. X7R/X5R: ±12.5% max. Y5V/Y5U/Z5U: ±30% max.</p> <p>Q for class 1 or DF for class 2 NPO: C 30pF , Q 200 C < 30pF , Q 100+10/3 C X7R/X5R: Rate Voltage 50V: 3.5% Rate Voltage 25V,16V: 5% (C<1uF) Rate Voltage 25V,16V: 7.5% (C 1uF) Rate Voltage 10V: 7.5% Y5V/Y5U/Z5U: Rate Voltage 25V: 7.5% Rate Voltage 16V: 10%(C<1 μ F) Rate Voltage 16V: 12.5%(C 1 μ F) Rate Voltage 10V: 15% I.R: More than 1000 M or 50 F min., whichever is smaller. Withstanding Voltage :No failure No remarkable damage</p>
<p>Endurance</p>	<p>Apply 200% of the rated voltage for 1000+24/-0 hours at the maximum operating temperature ±3 .</p> <p>Measurement to be made after keeping at room temperature for 24±2 hrs of class 1 part; for 48±4 hrs of class 2 part.</p>	<p>C/C: NPO: ±3% or ±0.3pF max. Whichever is larger. X7R/X5R: ±12.5% max. Y5V/Y5U/Z5U: ±30% max.</p> <p>Q for class 1 or DF for class 2 NPO: C 30pF , Q 350 10pF < C < 30pF , Q 275+5/2 C C 10pF , Q 200+10C X7R/X5R: Rate Voltage 50V: 3.5% Rate Voltage 25V,16V: 5% (C<1uF) Rate Voltage 25V,16V: 7.5% (C 1uF) Rate Voltage 10V: 7.5% Y5V/Y5U/Z5U: Rate Voltage 25V: 7.5% Rate Voltage 16V: 10%(C<1 μ F) Rate Voltage 16V: 12.5%(C 1 μ F) Rate Voltage 10V: 15% I.R: More than 1000 M or 50 F min., whichever is smaller. Withstanding Voltage :No failure No remarkable damage</p>

MULTILAYER CERAMIC CHIP CAPACITORS

PACKING

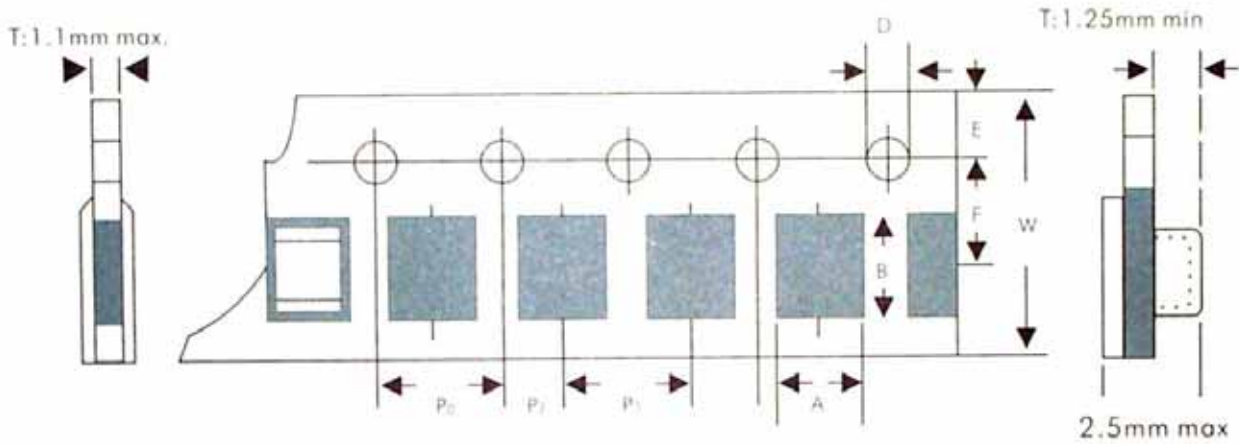


	Tape Size	A.	B Min.	C	D Min.	E Min.	W	T Max.
13" Reel	8mm	330±2 (12.99±0.08)	60 (2.362)	13.0±0.5 (0.51±0.02)	20.2 (0.795)	1.5 (0.059)	9±0.5 (0.35±0.02)	2.5 (0.1)
	12mm						13±0.5 (0.51±0.02)	
7" Reel	8mm	178±1 (7.01±0.04)	50 (1.969)	13.0±0.5 (0.51±0.02)	20.2 (0.795)	1.5 (0.059)	9±0.5 (0.35±0.02)	2.5 (0.1)
	12mm						13±0.5 (0.51±0.02)	

STANDARD

Size	7 Reel		13 Reel		Tape Width
	Paper	Plastic	Paper	Plastic	
0402	10,000	---	50,000	---	8mm
0603	4,000	---	15,000	---	
0805	4,000	3,000	10,000	10,000	
1206	4,000	3,000	10,000	10,000	
1210	---	3,000	---	---	12mm
1808	---	2,000 3,000	---	---	
1812	---	500 1,000	---	---	

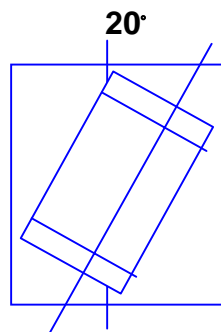
MULTILAYER CERAMIC CHIP CAPACITORS



	0402	0603	0805	1206	1210	1808	1812
A	0.62±0.05 (.024±.002)	1.1±0.2 (.043±.008)	1.5±0.2 (.059±.008)	1.9±0.2 (.075±.008)	2.8±0.2 (.110±.008)	2.3±0.2 (.091±.008)	3.5±0.2 (.138±.008)
B	1.15±0.1 (.045±.004)	1.9±0.2 (.075±.008)	2.3±0.2 (.091±.008)	3.5±0.2 (.138±.008)	3.5±0.2 (.138±.008)	4.9±0.2 (.193±.008)	4.9±0.2 (.193±.008)
D	1.5±0.1 (.059±.004)	1.5±0.1 (.059±.004)	1.5±0.1 (.059±.004)	1.5±0.1 (.059±.004)	1.5±0.1 (.059±.004)	1.5±0.1 (.059±.004)	1.5±0.1 (.059±.004)
E	1.75±0.1 (.069±.004)	1.75±0.1 (.069±.004)	1.75±0.1 (.069±.004)	1.75±0.1 (.069±.004)	1.75±0.1 (.069±.004)	1.75±0.1 (.069±.004)	1.75±0.1 (.069±.004)
F	3.5±0.1 (.138±.004)	3.5±0.1 (.138±.004)	3.5±0.1 (.138±.004)	3.5±0.1 (.138±.004)	3.5±0.1 (.138±.004)	5.5±0.1 (.217±.004)	5.5±0.1 (.217±.004)
P0	4.0±0.1 (.157±.004)	4.0±0.1 (.157±.004)	4.0±0.1 (.157±.004)	4.0±0.1 (.157±.004)	4.0±0.1 (.157±.004)	4.0±0.1 (.157±.004)	4.0±0.1 (.157±.004)
P1	4.0±0.1 (.157±.004)	4.0±0.1 (.157±.004)	4.0±0.1 (.157±.004)	4.0±0.1 (.157±.004)	4.0±0.1 (.157±.004)	4.0±0.1 (.157±.004)	4.0±0.1 (.157±.004)
P2	2.0±0.05 (.079±.002)	2.0±0.05 (.079±.002)	2.0±0.05 (.079±.002)	2.0±0.05 (.079±.002)	2.0±0.05 (.079±.002)	2.0±0.05 (.079±.002)	2.0±0.05 (.079±.002)
W	8.0±0.3 (.315±.012)	8.0±0.3 (.315±.012)	8.0±0.3 (.315±.012)	8.0±0.3 (.315±.012)	8.0±0.3 (.315±.012)	12.0±0.2 (.472±.008)	12.0±0.2 (.472±.008)

COMPONENT ROTATION

Maximum Component Rotation



Component
Center Line

Component
Cavity Center Line

MULTILAYER CERAMIC CHIP CAPACITORS

RESTRICTIVELY USED SUBSTANCES:

As the constituent table, no prohibited substances are used in Lian-Gimn parts.

We promised that Lian-Gimn deliver to Customer are free from any of the environmental hazardous substances. (The conditions and details are from customer's requirement and environment regulations.)

STORAGE CONDITION OF PRODUCTS:

Storage Environments.

Tape packing material are designed to withstand long-term storage, but they will degrade more rapidly in the presence of high temperature or high humidity, Therefore, the products must be stored in an ambient temperature of less than 40 with a relative humidity of less than 70%RH. Allowable storage period is within 12 months from the notice for final shipments.(As JEDEC Standard No. 48-A)

MULTILAYER CERAMIC CHIP CAPACITORS

The Essence of a capacitor

THE SORTS OF DIELECTRIC MATERIAL FROM THEIR COMPONENTS.

- 1) Ceramic
- 2) Tantalum
- 3) Electrolytic Aluminum
- 4) Polymer , OS- Con etc.

Different type of capacitor has its characteristics and suitable for specific applications ,but NOT for unspecified.

HOW IS A MULTI LAYER CERAMIC CAPACITOR FORMED

A number of conductive electrodes lay-down(Pd / Ag / Ni / Cu) separated by an insulating dielectric sheet

CAPACITORS IN SERIES

- 1) $1/C \text{ total} = 1/C_1 + 1/C_2 + 1/C_3 + \dots + 1/C_n$
- 2) Respective current equally.

CAPACITORS IN PARALLEL

- 3) $C \text{ total} = C_1 + C_2 + C_3 + \dots + C_n$
- 4) Respective voltage is equally.

STANDARD UNIT OF CAPACITANCE IS INDICATED AS "F OR FARAD"

$\mu\text{F} = \text{micro Farad} = 10^{-6}$

$\text{nF} = \text{nano Farad} = 10^{-9}$

$\text{pF} = \text{pico Farad} = 10^{-12}$

VOLTAGE AND AC

As a general rule, AC must not exceed 10% to the rated DC value.

If the AC voltage is too strong to the capacitor , the inner dielectric would heat-up and dissipation become an issue. Unusual AC spikes or surges will cause over heating and the dielectric would be ruptured or even on fire , This design rule should be strictly followed , particularly in the application above 1KHz switching frequency.

MULTILAYER CERAMIC CHIP CAPACITORS

THE PARASITICAL INDUCTANCE

Four contributed inductances

- 1) Component aspect ratio (chip length vs. width)
- 2) Circuit trace inductance
- 3) Via hole inductance
- 4) Packaging inductance

INDUCTIVE NOISE SUPPRESSION

When an inductor is inserted in series of a noise producing circuit, its impedance increases with frequency.

In this configuration, it is possible to attenuate and eliminate the noise components (high frequency components).

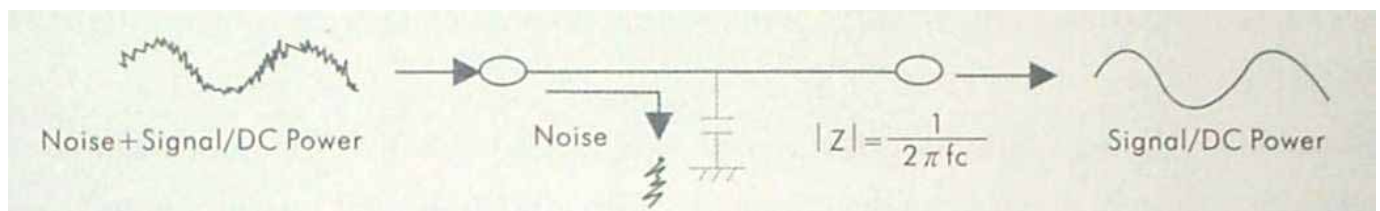


f : Frequency

L : Inductance value

CAPACITIVE NOISE SUPPRESSION

When a capacitor is connected (bypass capacitor) to ground from a noisy signal line or power line, the circuit impedance decreases as the frequency increases. Since noise is a high frequency phenomenon, it flows to ground. If a capacitor has been connected to ground, there by making it possible to eliminate noise.



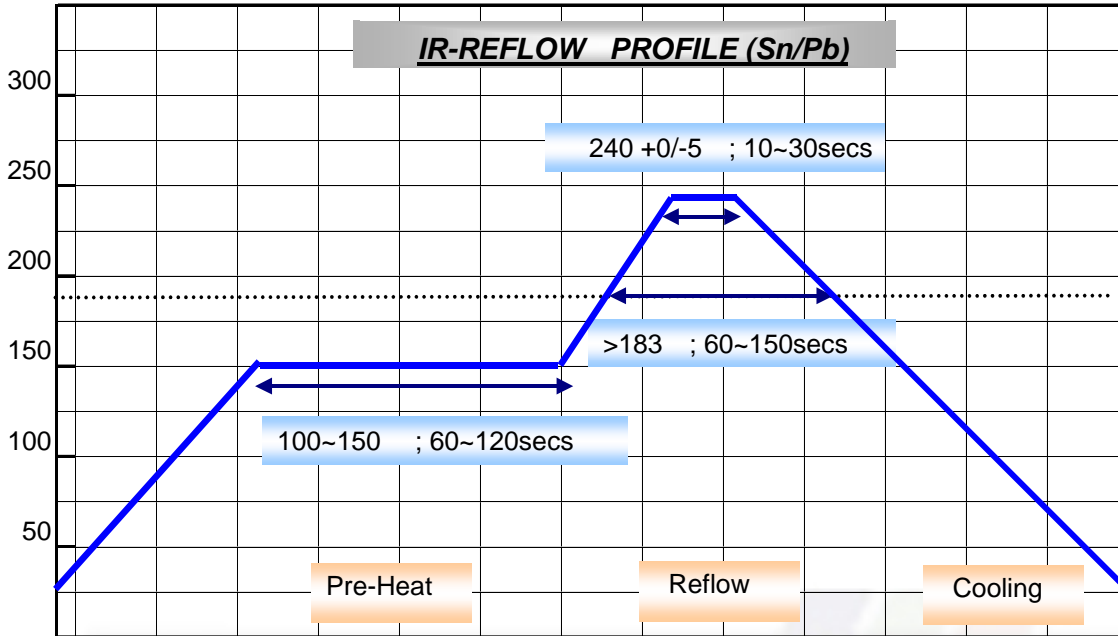
f : Frequency

c : Capacitor value

MULTILAYER CERAMIC CHIP CAPACITORS

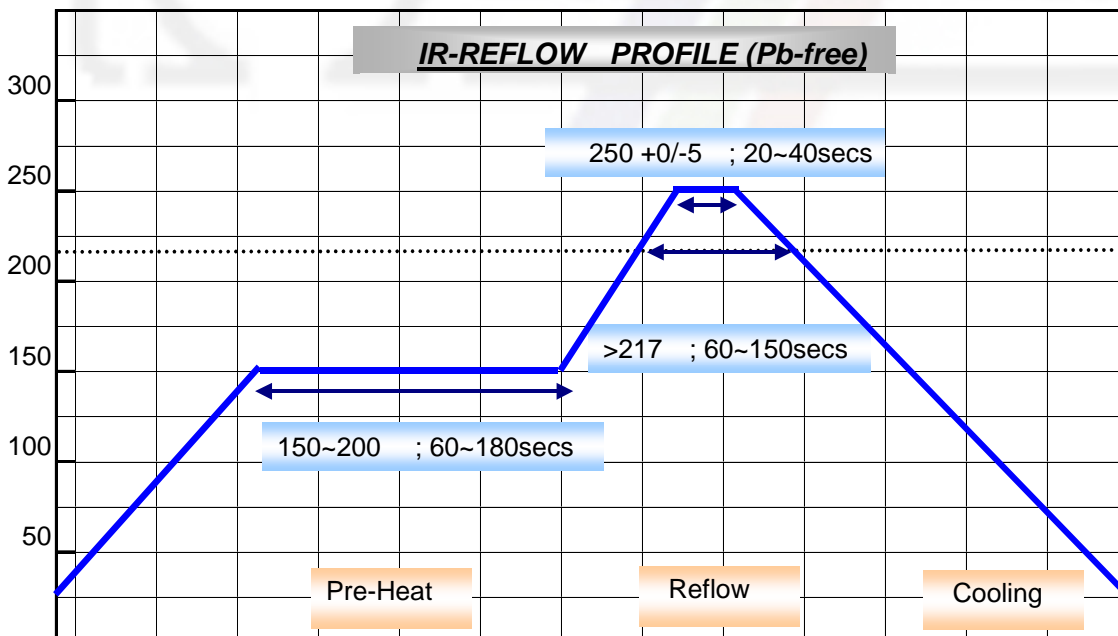
Soldering Recommendation

Typical Profile Band for Sn63/Pb37 Alloy Solder Paste



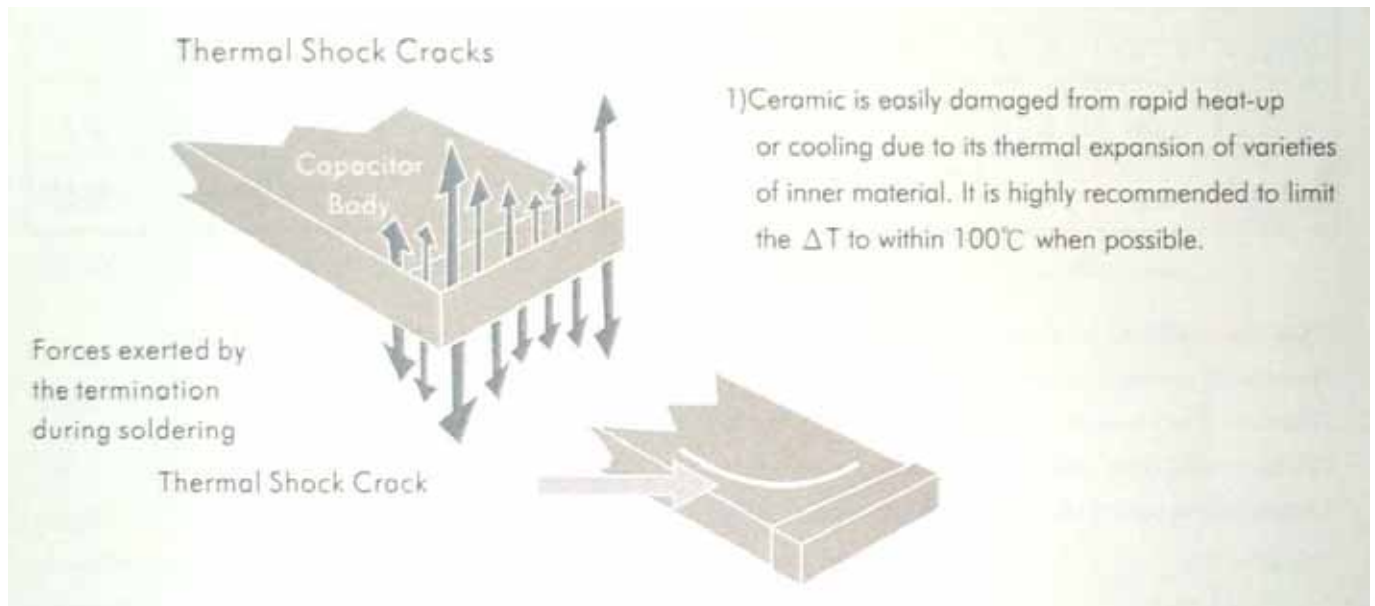
Soldering Recommendation

The IR-Reflow profile for lead free part.



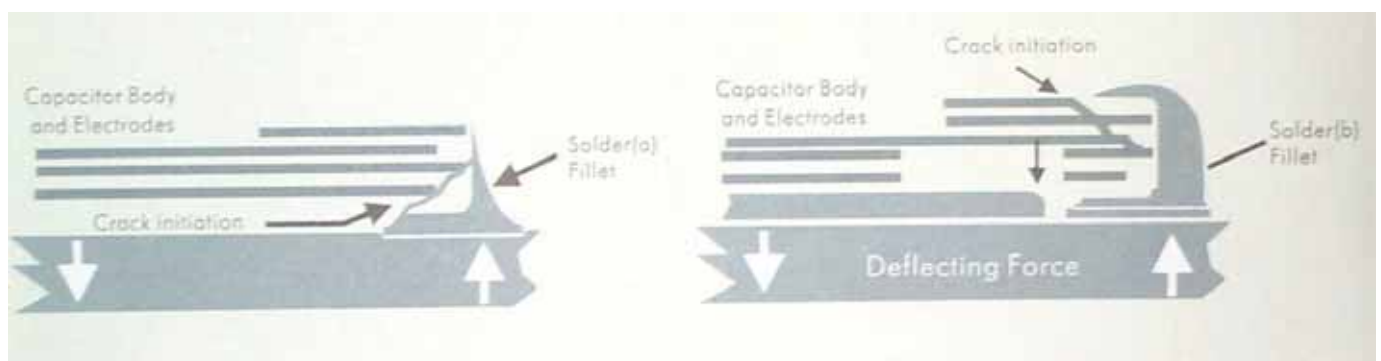
MULTILAYER CERAMIC CHIP CAPACITORS

THERMAL SHOCK



MECHANICAL DAMAGE

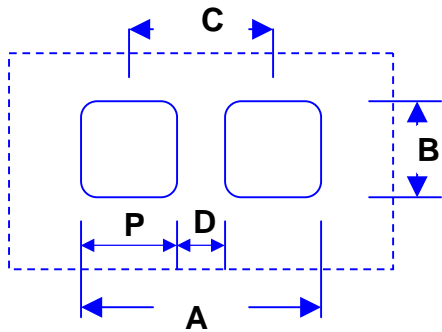
- 1) Board flexure cracks are common observed, especially manual breaking process is involved or large degree of PCB warpage exists at machine level handling.
- 2) The flexure crack can be eliminated by putting sensitive parts away from the high stress area. Position and orientation of the parts should be very important.



MULTILAYER CERAMIC CHIP CAPACITORS

SOLDER PAD DESIGN GUIDES

(in case more details required, please refer to IPC 782 A)



Unit: mm

Chip	IR Reflow					Wave Solder				
	A	D	B	P	C	A	D	B	P	C
*0402	1.70	0.50	0.50	0.60	1.10	N/A				
*0603	2.30	0.70	0.75	0.80	1.50	3.10	0.70	0.75	1.20	1.90
0805	3.00	1.00	1.25	1.00	2.00	4.10	1.00	1.25	1.50	2.50
1206	4.00	2.00	1.60	1.00	3.00	5.00	2.00	1.60	1.50	3.50
1210	4.00	2.00	2.50	1.00	3.00	5.00	2.00	2.50	1.50	3.50
1808	5.60	3.60	2.00	1.00	4.60	N/A				
1812	5.60	3.60	3.00	1.00	4.60	N/A				

Note:*to minimize tombstone for small chips 0402, 0603, four methodologies can be used

- 1) make all corners of the pads to round shape as above figure
- 2) Reduce the amount of solder paste using, a stencil opening which is less than the pad area
- 3) 130~160 pre-heating temperature for more than 1 minute
- 4) control the pad size as small as possible

MULTILAYER CERAMIC CHIP CAPACITORS

Terminology

CAPACITANCE:

$$C = \epsilon KA/t$$

CAPACITANCE TOLERANCE

is the amount of the actual capacitance allowed to deviate from the nominal value listed . For example , if you order a capacitor with a nominal of 1000pF and a tolerance of plus or minus 10%, you may get an actual value of 900 to 1100pF (at 25)

DISSIPATION FACTOR (DF OR TAN δ)

The amount of energy loss compared to that originally applied. DF is a measurement of how effective a capacitor is , $DF = ESR/X_c$

IRMS

Within a given temperature rise (10-20 , typical), the maximum allowable AC to flow through a capacitor , the higher Irms the better heat dissipation of the capacitor.

$$I_{rms} = \sqrt{P/ESR}$$

ESR

is accidentally built to non-ideal capacitor due to the material of inner electrodes and terminations .

$$ESR = DF/2\pi f_c$$

ESL

can also exists in non-ideal capacitor due to the aspect ratio (length vs. width of current path)

IZI

Is a combination of natural resistance and inductance properties . The total of these resistances is known as impedance. The amount of impedance to the current means determine it will pass or be blocked by the capacitor.

RATED VOLTAGE

All capacitors are rated for the amount of voltage which they can tolerate. By definition , voltage is the amount of pressure or force exerted on the current , to make the current move.

QUALITY FACTOR

Or "Q", is the reciprocal of DF. if Q is high , the capacitor is considered as more effectively.

MULTILAYER CERAMIC CHIP CAPACITORS

I . R.

Insulation Resistance comes from the dielectric and outer coating. If any, it is the only real resistance perceived by direct current , some DC leakage through the capacitor can occur . It depends on the capacitor's rating for IR . Ceramic Capacitors have relatively large IR ratings (1G or higher typically) than other dielectrics capacitor.

ALTERNATING CURRENT

AC is influenced by three resistances-ESR , inductance reactance X_L and capacitive reactance X_C . As a general rule , AC should not exceed 10% heat up and dissipation will become a problem ,this is a particular true for above 1KHZ.

SELF RESONANT FREQUENCY

When a capacitor reaches a certain frequency where the capacitive reactance X_C and inductance X_L cancel each other out, when X_C and X_L cancel, the only impedance left is ESR and the current easily passes along in the circuit.

DIELECTRIC STRENGTH

When a rated voltage is given in percents form and defined the upper limits of voltage. The ceramic dielectric can tolerate without rupturing. It is a test measure only and is applied to assure reliability and integrity of the capacitor . It does not guarantee proper capacitor performance and should not be used to choose a capacitor . Except for rated voltage being used.

PHASE ANGLE

$$\text{POWER FACTOR} = \cos \delta \quad \text{OR} \quad \sin \delta$$

$$\text{D.F.} = \tan \delta$$

